being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of forming a reflective mirror within a substrate, comprising the act of forming at least one empty-spaced pattern beneath a surface of and within said substrate, said empty-spaced pattern being positioned along an optical path of said substrate and being surrounded by substrate material.

2. The method of claim 1 further comprising the act of forming a plurality of empty-spaced patterns beneath said surface of said substrate, said empty-spaced patterns being sequentially positioned along said optical path of said substrate and being surrounded by said substrate material.

3. The method of claim 2, wherein said empty-spaced patterns are spaced apart to provide a predetermined refraction index corresponding to said substrate.

4. The method of claim 3, wherein said empty-spaced patterns are spaced apart uniformly.

5. The method of claim 3, wherein said empty-spaced patterns are spaced apart nonuniformly.

6. The method of claim 3, wherein said empty-spaced patterns are spaced apart to provide a maximum reflectivity value corresponding to maximum electromagnetic wave reflection for said reflective mirror.

7. The method of claim 2, wherein said act of forming said empty-spaced patterns further comprises forming a plurality of holes within said substrate and annealing said substrate to form said empty-spaced patterns beneath said surface of said material.

8. The method of claim 7, wherein said holes are cylindrical holes.

9. The method of claim 7, wherein said substrate is annealed at a temperature lower than a melting temperature of said substrate material.

10. The method of claim 9, wherein said substrate is annealed under a hydrogen ambient.

11. The method of claim 9, wherein said substrate is annealed for about 60 seconds.

12. The method of claim 2, wherein at least one of said empty-spaced patterns has a plate-shaped configuration.

13. The method of claim 2, wherein said empty-spaced patterns are plate-shaped empty-spaced patterns.

14. The method of claim 13, wherein said plate-shaped empty-spaced patterns have same thicknesses.

15. The method of claim 13, wherein said plate-shaped empty-spaced patterns have different thicknesses.

16. The method of claim 2, wherein said empty-spaced patterns are formed simultaneously.

17. The method of claim 2, wherein said substrate is a monocrystalline substrate.

18. The method of claim 17, wherein said substrate is a silicon substrate.

19. The method of claim 17, wherein said substrate is a quartz substrate.

20. The method of claim 17, wherein said substrate is a germanium substrate.

21. The method of claim 2, wherein said substrate is a gallium arsenide substrate.

22. The method of claim 2, wherein said substrate is an indium gallium arsenide substrate.

23. A method of modifying the transmission of an electromagnetic wave, said method comprising the steps of:

transmitting said electromagnetic wave through a monocrystalline substrate, said monocrystalline substrate comprising at least one plate-shaped empty spaced pattern within, and surrounded by, said monocrystalline substrate, and below a surface of said monocrystalline substrate, said at least one plate-shaped empty spaced pattern being positioned along a transmission axis of said electromagnetic wave; and

phase-shifting said electromagnetic wave as it passes through said monocrystalline substrate.

24. The method of claim 23, wherein said electromagnetic wave is phase-shifted about 180 degrees.

25. The method of claim 23 further comprising the act of forming at least one hole within said monocrystalline substrate and annealing said monocrystalline substrate to form said at least one plate-shaped empty spaced pattern beneath said surface of said monocrystalline substrate.

26. The method of claim 25, wherein said act of annealing is performed under a reducing atmosphere.

27. The method of claim 26, wherein said reducing atmosphere is a hydrogen atmosphere at a temperature lower than the melting temperature of said monocrystalline substrate.

28. The method of claim 23 further comprising the act of forming at least two plate-shaped empty spaced patterns positioned along said transmission axis of said electromagnetic wave.

29. The method of claim 28, wherein said at least two plate-shaped empty spaced patterns are formed sequentially.

30. The method of claim 28, wherein said at least two plate-shaped empty spaced patterns are formed simultaneously.

31. The method of claim 30, wherein one of said plate-shaped empty spaced patterns is located below said other plate-shaped empty spaced pattern relative to said surface of said monocrystalline substrate.

32. The method of claim 30, wherein said plate-shaped empty spaced patterns have same thicknesses.

33. The method of claim 30, wherein said plate-shaped empty spaced patterns have different thicknesses.

34. The method of claim 23, wherein said monocrystalline substrate is a germanium substrate.

35. The method of claim 23, wherein said monocrystalline substrate is a silicon substrate.

36. The method of claim 23, wherein said monocrystalline substrate is a silicon-on-insulator substrate.

37. The method of claim 23, wherein said monocrystalline substrate is a silicon-on-nothing substrate.

38. The method of claim 23, wherein said monocrystalline substrate is a gallium arsenide substrate.

39. A method of forming a reflective mirror within a substrate, said method comprising the acts of:

forming a plurality of cylindrical holes within said substrate, each of said plurality of cylindrical holes being defined by a radius $R = \lambda/4\ [(2k+1)/n + (2m+1)]\ (1/8.89)$, wherein λ is a wavelength for which the reflectivity of said reflective mirror is maximum, n is the refraction index of said substrate, and k and m are real integers, and wherein any two adjacent cylindrical holes are spaced apart by a distance $\Delta_N^2 = 27.83\ R^3/\ (2m+1)\ \lambda/4$; and

annealing said substrate to form at least one empty-spaced pattern beneath a surface of and within said substrate, said empty-spaced pattern being positioned along an optical path of said substrate.

40. The method of claim 39 further comprising the act of forming a plurality of empty-spaced patterns beneath said surface of said substrate, said empty-spaced patterns being sequentially positioned along said optical path of said substrate and being surrounded by substrate material.

41. The method of claim 40, wherein said substrate is annealed at a temperature lower than a melting temperature of said substrate.

42. The method of claim 41, wherein said substrate is annealed under a hydrogen ambient.

43. The method of claim 40, wherein said empty-spaced patterns are plate-shaped empty-spaced patterns.

44. The method of claim 43, wherein said plate-shaped empty-spaced patterns have same thicknesses.

45. The method of claim 43, wherein said plate-shaped empty-spaced patterns have different thicknesses.

46. The method of claim 43, wherein said plate-shaped empty-spaced patterns are formed simultaneously.

47. The method of claim 43, wherein said plate-shaped empty-spaced patterns are spaced apart uniformly.

48. The method of claim 43, wherein said plate-shaped empty-spaced patterns are spaced apart non-uniformly.

49. The method of claim 40, wherein said substrate is a monocrystalline substrate.

50. The method of claim 49, wherein said substrate is a silicon substrate.

51. The method of claim 49, wherein said substrate is a quartz substrate.

52. The method of claim 49, wherein said substrate is a germanium substrate.

53. The method of claim 40, wherein said substrate is a gallium arsenide substrate.

54. The method of claim 40, wherein said substrate is an indium gallium arsenide substrate.

55. An integrated circuit substrate comprising at least one reflective mirror provided beneath a surface of, and within, a semiconductor substrate, said reflective mirror comprising at least one empty-spaced pattern beneath said surface of and within said substrate, said at least one empty-spaced pattern being positioned along an optical path of said substrate and being surrounded by substrate material.

56. The integrated circuit of claim 55 further comprising a plurality of empty-spaced patterns beneath said surface of and within said substrate, said empty-spaced patterns being sequentially positioned along said optical path of said substrate and being surrounded by said substrate material.

57. The integrated circuit of claim 56, wherein said plurality of empty-spaced patterns are spaced apart uniformly.

58. The integrated circuit of claim 56, wherein said plurality of empty-spaced patterns are spaced apart non-uniformly.

59. The integrated circuit of claim 56, wherein each of said plurality of empty-spaced patterns has a respective refraction index.

60. The integrated circuit of claim 56, wherein said plurality of empty-spaced patterns has a maximum reflectivity value corresponding to maximum electromagnetic wave reflection for said reflective mirror.

61. The integrated circuit of claim 56, wherein said empty-spaced patterns are plate-shaped empty-spaced patterns.

62. The integrated circuit of claim 61, wherein said plate-shaped empty-spaced patterns have same thicknesses.

63. The integrated circuit of claim 61, wherein said plate-shaped empty-spaced patterns have different thicknesses.

64. The integrated circuit of claim 56, wherein said semiconductor substrate is a silicon substrate.

65. The integrated circuit of claim 56, wherein said semiconductor substrate is a quartz substrate.

66. The integrated circuit of claim 56, wherein said semiconductor substrate is a germanium substrate.

67. The integrated circuit of claim 56, wherein said semiconductor substrate is a silicon-on-insulator substrate.

68. The integrated circuit of claim 56, wherein said semiconductor substrate is a silicon-on-nothing substrate.

69. The integrated circuit of claim 56, wherein said semiconductor substrate includes a laser.

70. The integrated circuit of claim 69, wherein said laser is a vertical cavity laser and said reflective mirror being is located below a junction of said vertical cavity laser.

71. The integrated circuit of claim 69, wherein said laser is a solid state ion laser, said reflective mirror being embedded within at least one end face of such solid state ion laser.

72. A laser device comprising a laser body for producing laser light and at least one mirror coupled to said laser body to reflect said laser light, said at least one mirror comprising at least one empty-spaced pattern beneath a surface of and within a substrate, said empty-spaced pattern being positioned along an optical path of said laser device and being surrounded by substrate material.

73. The laser device of claim 72, wherein said at least one mirror further comprises a plurality of empty-spaced patterns beneath said surface of and within said substrate, said empty-spaced patterns being sequentially positioned along said optical path of said laser device and being surrounded by said substrate material.

74. The laser device of claim 73, wherein said plurality of empty-spaced patterns are spaced apart uniformly.

75. The laser device of claim 73, wherein said plurality of empty-spaced patterns are spaced apart non-uniformly.

76. The laser device of claim 73, wherein each of said plurality of empty-spaced patterns has a respective refraction index.

77. The laser device of claim 73, wherein said plurality of empty-spaced patterns has a maximum reflectivity value corresponding to maximum laser wave reflection for said reflective mirror.

78. The laser device of claim 73, wherein said empty-spaced patterns are plate-shaped empty-spaced patterns.

79. The laser device of claim 78, wherein said plate-shaped empty-spaced patterns have same thicknesses.

80. The laser device of claim 78, wherein said plate-shaped empty-spaced patterns have different thicknesses.

81. The laser device of claim 72 further comprising at least two said mirrors coupled to opposite sides of said laser body to reflect said laser light.